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EXAMINER	
PUENTE, EMERSON C	
ART UNIT	**PAPER NUMBER**
2113	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/621,945	VAIDYANATHAN, BASU	
	Examiner	Art Unit	
	Emerson C. Puente	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is made **Non-Final**.

Claims 1-21 have been examined.

Claim Objections

Claims 1,8,9,11,12,14,15, and 21 are objected to because of the following informalities:

In regards to claims 1, 8, and 15, please change "assigning the spare processor to replace failed processor" to "assigning the spare processor to replace **the** failed processor" (see last two line of claims).

In regards to claim 8, please change "identifying"(see lines 5-6 of claim) to "identifying means for identifying" to maintain consistent language.

In regards to claim 9 and 11, please change "claim 8, marking means" to "claim 8, **comprising** marking means"(see lines 1-2 of claims).

In regards to claim 12, please remove redundant limitation "in a data processing system"(see lines 1-2 of claim). Furthermore, please change "identifying"(see line 7 of claim) to "identifying means for identifying" to maintain consistent language.

In regards to claims 14 and 21, please change "filed processor" to "failed processor" (see last line of claims).

In regards to claim 15, please change "second instructions assigning" to "second instructions **for** assigning" (see line 8 of claim).

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 15-21 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

In regards to claims 15-21, the claimed "computer readable medium" as described in the specification page(s) 20, lines 2-5, includes, among other examples, transmission-type media, such as digital and analog communication links, wired or wireless communications links using transmission forms, such as, for example, radio frequency and light wave transmission, which is nonstatutory. As such, the claim is not limited to statutory subject matter and is therefore non-statutory.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1,2,8,9,15, and 16 rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 7,017,074 of Okin referred hereinafter "Okin".

In regards to claim 1, Okin discloses a method in a multi-processor data processing system for managing processors, the method comprising:

responsive to detecting a failed processor in a set of processors on a multi-chip module, identifying a spare processor on the multi-chip module and assigning the spare processor to replace failed processor. Okin discloses bring a processor into operation, substituting for the failed processor (see column 3 lines 23-24). Okin further discloses wherein the processors are formed on a die, and hence on the chip (see column 2 lines 32-35).

In regards to claim 2, Okin discloses the claim limitations as disclosed above. Okin further discloses wherein the spare processor on the multi-chip module is marked for use as a spare. Okin discloses one processor is not being used when other processors are operational and upon failure to one of the processors, bring the processor into operation, substituting for the failed one (see column 3 lines 10-13 and 23-24).

In regards to claim 8, Okin discloses a multi-processor data processing system for managing processors, the data processing system comprising:

detecting means for detecting a failed processor in a set of processors on a multi-chip module, identifying a spare processor on the multi-chip module and assigning means for assigning the spare processor to replace failed processor. Okin discloses bring a processor into operation, substituting for the failed processor (see column 3 lines 23-24). Okin further discloses wherein the processors are formed on a die, and hence on the chip (see column 2 lines 32-35).

In regards to claim 9, Okin discloses the claim limitations as disclosed above. Okin further discloses marking means for marking the spare processor on the multi-chip module for use as a spare. Okin discloses one processor is not being used when other processors are operational and upon failure to one of the processors, bring the processor into operation, substituting for the failed one (see column 3 lines 10-13 and 23-24).

In regards to claim 15, Okin discloses a computer program product in a computer readable medium for managing processors, the computer program product comprising:

first instructions responsive to detecting a failed processor in a set of processors on a multi-chip module, identifying a spare processor on the multi-chip module and second instructions assigning the spare processor to replace failed processor. Okin discloses bring a processor into operation, substituting for the failed processor (see column 3 lines 23-24). Okin further discloses wherein the processors are formed on a die, and hence on the chip (see column 2 lines 32-35).

In regards to claim 16, Okin discloses the claim limitations as disclosed above. Okin further discloses wherein the spare processor on the multi-chip module is marked for use as a spare. Okin discloses one processor is not being used when other processors are operational and upon failure to one of the processors, bring the processor into operation, substituting for the failed one (see column 3 lines 10-13 and 23-24).

Claims 5,12, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,485,604 of Miyoshi et al. referred hereinafter "Miyoshi".

In regards to claim 5, Miyoshi discloses a method in a data processing system for managing processors, the method comprising:

monitoring for a failed processor in the processors. Miyoshi discloses detecting faults in active central processor modules (see column 3 lines 14-16).

responsive to detecting a failed processor, identifying a spare processor from a set of spare processors, wherein the set of spare processors are located on different modules and wherein the spare processor is identified as minimizing degradation in processing performance. Miyoshi discloses in the event an active processor fails, one of the standby central processing modules is selected as substitute (see column 3 lines 26-29).

In regards to claim 12, Miyoshi discloses a multi-processor data processing system in a data processing system for managing processors, the data processing system comprising:

monitoring means for monitoring for a failed processor in the processors. Miyoshi discloses detecting faults in active central processor modules (see column 3 lines 14-16).

detecting means for detecting a failed processor, identifying a spare processor from a set of spare processors, wherein the set of spare processors are located on different modules and wherein the spare processor is identified as minimizing degradation in processing performance. Miyoshi discloses in the event an active processor fails, one of the standby central processing modules is selected as substitute (see column 3 lines 26-29).

In regards to claim 19, Miyoshi discloses a computer program product in a computer readable medium in a data processing system for managing processors, the computer program product comprising:

rirst instructions for monitoring for a failed processor in the processors. Miyoshi discloses detecting faults in active central processor modules (see column 3 lines 14-16).

second instructions responsive to detecting a failed processor, identifying a spare processor from a set of spare processors, wherein the set of spare processors are located on different modules and wherein the spare processor is identified as minimizing degradation in processing performance. Miyoshi discloses in the event an active processor fails, one of the standby central processing modules is selected as substitute (see column 3 lines 26-29).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3,6-10,13-17,20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyoshi view Okin.

In regards to claim 1, Miyoshi discloses a method in a multi-processor data processing system for managing processors, the method comprising:

responsive to detecting a failed processor in a set of processors on a multi-chip module, identifying a spare processor and assigning the spare processor to replace failed processor. Miyoshi discloses in the event an active processor fails, one of the standby central processing modules is selected as substitute (see column 3 lines 26-29).

However, Miyoshi fails to discloses:

wherein the spare processor is on the multi-chip module.

Okin discloses a processor module comprising a plurality of processors, wherein one of the processor substitutes for a failed processor (see column 3 lines 10-13 and 23-24), indicating wherein the spare processor is on the multi-chip module.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Miyoshi and Okin such that each of the processor modules, as disclosed in Miyoshi, include a plurality of processors, wherein one of the processor substitutes for a failed processor, indicating wherein the spare processor is on the multi-chip module. A person of ordinary skill in the art would have been motivated to combine the teachings because Miyoshi is concerned with providing a fault tolerant computer system (see column 1 lines 55-56 and column 2 lines 58-65) and having a processor module comprising a plurality of processors, wherein one of the processor substitutes for a failed processor, as per teachings of Okin, provides greater reliability (see column 2 lines 5-10) and hence, a greater level of fault tolerance.

In regards to claim 2, Miyoshi in view of Okin discloses the claim limitations as disclosed above. Okin further discloses wherein the spare processor on the multi-chip module is marked for use as a spare. Okin discloses one processor is not being used when other processors are operational and upon failure to one of the processors, bring the processor into operation, substituting for the failed one (see column 3 lines 10-13 and 23-24).

In regards to claim 3, Miyoshi in view of Okin discloses the claim limitations as disclosed above. Miyoshi further discloses selecting another spare processor on a different multi-chip module if the spare processor is absent. Miyoshi discloses in the event an active processor

fails, one of the standby central processing modules is selected as substitute (see column 3 lines 26-29).

In regards to claim 6, Miyoshi discloses all the claim limitation as disclosed above. However, Miyoshi fails to explicitly disclose:

wherein the spare processor is selected from a module containing the failed processor.

Okin discloses a processor module comprising a plurality of processors, wherein one of the processor substitutes for a failed processor (see column 3 lines 10-13 and 23-24), indicating selecting a spare processor from a module containing the failed processor.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Miyoshi and Okin such that each of the processor modules, as disclosed in Miyoshi, include a plurality of processors, wherein one of the processor substitutes for a failed processor, indicating wherein the spare processor is selected from a module containing the failed processor. A person of ordinary skill in the art would have been motivated to combine the teachings because Miyoshi is concerned with providing a fault tolerant computer system (see column 1 lines 55-56 and column 2 lines 58-65) and having a processor module comprising a plurality of processors, wherein one of the processor substitutes for a failed processor, as per teachings of Okin, provides greater reliability (see column 2 lines 5-10) and hence, a greater level of fault tolerance.

In regards to claim 7, Miyoshi in view of Okin discloses the claim limitations as disclosed above. Okin further discloses wherein the spare processor is selected from a die containing the failed processor. Okin discloses wherein the processors are formed on a die (see column 2 lines 32-35).

In regards to claim 8, Miyoshi discloses a multi-processor data processing system for managing processors, the data processing system comprising:

detecting means for detecting a failed processor in a set of processors on a multi-chip module, identifying a spare processor and assigning means for assigning the spare processor to replace failed processor. Miyoshi discloses in the event an active processor becomes faulty, one of the standby central processing modules is selected as substitute (see column 3 lines 26-29).

However, Miyoshi fails to discloses:

wherein the spare processor is on the multi-chip module.

Okin discloses a processor module comprising a plurality of processors, wherein one of the processor substitutes for a failed processor (see column 3 lines 10-13 and 23-24), indicating wherein the spare processor is on the multi-chip module.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Miyoshi and Okin such that each of the processor modules, as disclosed in Miyoshi, include a plurality of processors, wherein one of the processor substitutes for a failed processor, indicating wherein the spare processor is on the multi-chip module. A person of ordinary skill in the art would have been motivated to combine the teachings because Miyoshi is concerned with providing a fault tolerant computer system (see column 1 lines 55-56 and column 2 lines 58-65) and having a processor module comprising a plurality of processors, wherein one of the processor substitutes for a failed processor, as per teachings of Okin, provides greater reliability (see column 2 lines 5-10) and hence, a greater level of fault tolerance.

In regards to claim 9, Miyoshi in view of Okin discloses the claim limitations as disclosed above. Okin further discloses marking means for marking the spare processor on the multi-chip module for use as a spare. Okin discloses one processor is not being used when other processors are operational and upon failure to one of the processors, bring the processor into operation, substituting for the failed one (see column 3 lines 10-13 and 23-24).

In regards to claim 10, Miyoshi in view of Okin discloses the claim limitations as disclosed above. Miyoshi further discloses selecting means for selecting another spare processor on a different multi-chip module if the spare processor is absent. Miyoshi discloses in the event an active processor becomes faulty, one of the standby central processing modules is selected as substitute (see column 3 lines 26-29).

In regards to claim 13, Miyoshi discloses all the claim limitation as disclosed above. However, Miyoshi fails to explicitly disclose:

selecting means for selecting the spare processor from a module containing the failed processor.

Okin discloses a processor module comprising a plurality of processors, wherein one of the processor substitutes for a failed processor (see column 3 lines 10-13 and 23-24), indicating selecting a spare processor from a module containing the failed processor.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Miyoshi and Okin such that each of the processor modules, as disclosed in Miyoshi, include a plurality of processors, wherein one of the processor substitutes for a failed processor, indicating selecting means for selecting the spare processor from a module containing the failed processor. A person of ordinary skill in the art would have

been motivated to combine the teachings because Miyoshi is concerned with providing a fault tolerant computer system (see column 1 lines 55-56 and column 2 lines 58-65) and having a processor module comprising a plurality of processors, wherein one of the processor substitutes for a failed processor, as per teachings of Okin, provides greater reliability (see column 2 lines 5-10) and hence, a greater level of fault tolerance.

In regards to claim 14, Miyoshi in view of Okin discloses the claim limitations as disclosed above. Okin further discloses selecting means for selecting the spare processor from a die containing the failed processor. Okin discloses wherein the processors are formed on a die (see column 2 lines 32-35).

In regards to claim 15, Miyoshi discloses a computer program product in a computer readable medium for managing processors, the computer program product comprising:

first instructions responsive to detecting a failed processor in a set of processors on a multi-chip module, identifying a spare processor and second instructions assigning the spare processor to replace failed processor. Miyoshi discloses in the event an active processor becomes faulty, one of the standby central processing modules is selected as substitute (see column 3 lines 26-29).

However, Miyoshi fails to discloses:

wherein the spare processor is on the multi-chip module.

Okin discloses a processor module comprising a plurality of processors, wherein one of the processor substitutes for a failed processor (see column 3 lines 10-13 and 23-24), indicating wherein the spare processor is on the multi-chip module.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Miyoshi and Okin such that each of the processor modules, as disclosed in Miyoshi, include a plurality of processors, wherein one of the processor substitutes for a failed processor, indicating wherein the spare processor is on the multi-chip module. A person of ordinary skill in the art would have been motivated to combine the teachings because Miyoshi is concerned with providing a fault tolerant computer system (see column 1 lines 55-56 and column 2 lines 58-65) and having a processor module comprising a plurality of processors, wherein one of the processor substitutes for a failed processor, as per teachings of Okin, provides greater reliability (see column 2 lines 5-10) and hence, a greater level of fault tolerance.

In regards to claim 16, Miyoshi in view of Okin discloses the claim limitations as disclosed above. Okin further discloses wherein the spare processor on the multi-chip module is marked for use as a spare. Okin discloses one processor is not being used when other processors are operational and upon failure to one of the processors, bring the processor into operation, substituting for the failed one (see column 3 lines 10-13 and 23-24).

In regards to claim 17, Miyoshi in view of Okin discloses the claim limitations as disclosed above. Miyoshi further discloses third instructions for selecting another spare processor on a different multi-chip module if the spare processor is absent. Miyoshi discloses in the event an active processor becomes faulty, one of the standby central processing modules is selected as substitute (see column 3 lines 26-29).

In regards to claim 20, Miyoshi discloses all the claim limitation as disclosed above. However, Miyoshi fails to explicitly disclose:

wherein the spare processor is selected from a module containing the failed processor.

Okin discloses a processor module comprising a plurality of processors, wherein one of the processor substitutes for a failed processor (see column 3 lines 10-13 and 23-24), indicating selecting a spare processor from a module containing the failed processor.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Miyoshi and Okin such that each of the processor modules, as disclosed in Miyoshi, include a plurality of processors, wherein one of the processor substitutes for a failed processor, indicating wherein the spare processor is selected from a module containing the failed processor. A person of ordinary skill in the art would have been motivated to combine the teachings because Miyoshi is concerned with providing a fault tolerant computer system (see column 1 lines 55-56 and column 2 lines 58-65) and having a processor module comprising a plurality of processors, wherein one of the processor substitutes for a failed processor, as per teachings of Okin, provides greater reliability (see column 2 lines 5-10) and hence, a greater level of fault tolerance.

In regards to claim 21, Miyoshi in view of Okin discloses the claim limitations as disclosed above. Okin further discloses wherein the spare processor is selected from a die containing the failed processor. Okin discloses wherein the processors are formed on a die (see column 2 lines 32-35).

Claims 4,11, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okin in view US Patent No. 5,867,658 of Lee and US Patent No. 5,802,365 of Kathail et al. referred hereinafter "Kathail".

In regards to claim 4, Okin discloses the claim limitation as disclosed above. However, Okin fails to explicit disclose:

wherein the spare processor is marked by an open firmware.

Lee discloses it is conventional to operate open firmware in a multiprocessor-based system (see column 1 lines 26-29).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Okin and Lee to operate open firmware. A person of ordinary skill in the art would have been motivated to combine the teachings because Okin discloses using firmware (see column 2 lines 49) in a multiprocessor system (see column 6 line 55) and open firmware, as per teachings of Lee, constitutes firmware commonly known and used within microprocessor systems (see column 6 lines 26-29).

Furthermore, Kathail discloses creating a device tree, describing the hardware devices in the computer system with open firmware (see column 25 lines 33-35). Since open firmware describes the hardware devices in the computer system, it would identify or mark the spare processor.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Okin, Lee, and Kathail to create a device tree describing the hardware devices in the computer system with the open firmware, thus indicating marking the spare processor by an open firmware. A person of ordinary skill in the art would have been motivated to combine the teachings because Lee discloses using open firmware (see column 1 lines 26-29) and Kathail discloses a device tree is a known feature of open firmware (see column 25 lines 33-35).

In regards to claim 11, Okin discloses the claim limitation as disclosed above. However, Okin fails to explicit disclose:

marking means for marking the spare processor by an open firmware.

Lee discloses it is conventional to operate open firmware in a multiprocessor-based system (see column 1 lines 26-29).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Okin and Lee to operate open firmware. A person of ordinary skill in the art would have been motivated to combine the teachings because Okin discloses using firmware (see column 2 lines 49) in a multiprocessor system (see column 6 line 55) and open firmware, as per teachings of Lee, constitutes firmware commonly known and used within microprocessor systems (see column 6 lines 26-29).

Furthermore, Kathail discloses creating a device tree, describing the hardware devices in the computer system with open firmware (see column 25 lines 33-35). Since open firmware describes the hardware devices in the computer system, it would identify or mark the spare processor.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Okin, Lee, and Kathail to create a device tree describing the hardware devices in the computer system with the open firmware, thus indicating marking means for marking the spare processor by an open firmware. A person of ordinary skill in the art would have been motivated to combine the teachings because Lee discloses using open firmware (see column 1 lines 26-29) and Kathail discloses a device tree is a known feature of open firmware (see column 25 lines 33-35).

In regards to claim 18, Okin discloses the claim limitation as disclosed above. However, Okin fails to explicit disclose:

wherein the spare processor is marked by an open firmware.

Lee discloses it is conventional to operate open firmware in a multiprocessor-based system (see column 1 lines 26-29).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Okin and Lee to operate open firmware. A person of ordinary skill in the art would have been motivated to combine the teachings because Okin discloses using firmware (see column 2 lines 49) in a multiprocessor system (see column 6 line 55) and open firmware, as per teachings of Lee, constitutes firmware commonly known and used within microprocessor systems (see column 6 lines 26-29).

Furthermore, Kathail discloses creating a device tree, describing the hardware devices in the computer system with open firmware (see column 25 lines 33-35). Since open firmware describes the hardware devices in the computer system, it would identify or mark the spare processor.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Okin, Lee, and Kathail to create a device tree describing the hardware devices in the computer system with the open firmware, thus indicating marking the spare processor by an open firmware. A person of ordinary skill in the art would have been motivated to combine the teachings because Lee discloses using open firmware (see column 1 lines 26-29) and Kathail discloses a device tree is a known feature of open firmware (see column 25 lines 33-35).

Claims 4, 11, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyoshi in view of Okin and in further view of Lee and Kathail

In regards to claim 4, Miyoshi in view of Okin discloses the claim limitation as disclosed above. However, Miyoshi in view of Okin fails to explicit disclose:

wherein the spare processor is marked by an open firmware.

Lee discloses it is conventional to operate open firmware in a multiprocessor-based system (see column 1 lines 26-29).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Miyoshi, Okin and Lee to operate open firmware. A person of ordinary skill in the art would have been motivated to combine the teachings because Miyoshi in view of Okin discloses using firmware (see column 2 lines 49 of Okin) in a multiprocessor system (see column 6 line 55 of Okin and column 2 lines 60-65 of Miyoshi) and open firmware, as per teachings of Lee, constitutes firmware commonly known and used within microprocessor systems (see column 6 lines 26-29).

Furthermore, Kathail discloses creating a device tree, describing the hardware devices in the computer system with open firmware (see column 25 lines 33-35). Since open firmware describes the hardware devices in the computer system, it would identify or mark the spare processor.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Miyoshi, Okin, Lee, and Kathail to create a device tree describing the hardware devices in the computer system with the open firmware, thus indicating

marking the spare processor by an open firmware. A person of ordinary skill in the art would have been motivated to combine the teachings because Lee discloses using open firmware (see column 1 lines 26-29) and Kathail discloses a device tree is a known feature of open firmware (see column 25 lines 33-35).

In regards to claim 11, Miyoshi in view of Okin discloses the claim limitation as disclosed above. However, Miyoshi in view of Okin fails to explicit disclose:

marking means for marking the spare processor by an open firmware.

Lee discloses it is conventional to operate open firmware in a multiprocessor-based system (see column 1 lines 26-29).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Miyoshi, Okin and Lee to operate open firmware. A person of ordinary skill in the art would have been motivated to combine the teachings because Miyoshi in view of Okin discloses using firmware (see column 2 lines 49 of Okin) in a multiprocessor system (see column 6 line 55 of Okin and column 2 lines 60-65 of Miyoshi) and open firmware, as per teachings of Lee, constitutes firmware commonly known and used within microprocessor systems (see column 6 lines 26-29).

Furthermore, Kathail discloses creating a device tree, describing the hardware devices in the computer system with open firmware (see column 25 lines 33-35). Since open firmware describes the hardware devices in the computer system, it would identify or mark the spare processor.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Miyoshi, Okin, Lee, and Kathail to create a device tree

describing the hardware devices in the computer system with the open firmware, thus indicating marking means for marking the spare processor by an open firmware. A person of ordinary skill in the art would have been motivated to combine the teachings because Lee discloses using open firmware (see column 1 lines 26-29) and Kathail discloses a device tree is a known feature of open firmware (see column 25 lines 33-35).

In regards to claim 18, Miyoshi in view of Okin discloses the claim limitation as disclosed above. However, Miyoshi in view of Okin fails to explicit disclose:

wherein the spare processor is marked by an open firmware.

Lee discloses it is conventional to operate open firmware in a multiprocessor-based system (see column 1 lines 26-29).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Miyoshi, Okin and Lee to operate open firmware. A person of ordinary skill in the art would have been motivated to combine the teachings because Miyoshi in view of Okin discloses using firmware (see column 2 lines 49 of Okin) in a multiprocessor system (see column 6 line 55 of Okin and column 2 lines 60-65 of Miyoshi) and open firmware, as per teachings of Lee, constitutes firmware commonly known and used within microprocessor systems (see column 6 lines 26-29).

Furthermore, Kathail discloses creating a device tree, describing the hardware devices in the computer system with open firmware (see column 25 lines 33-35). Since open firmware describes the hardware devices in the computer system, it would identify or mark the spare processor.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Miyoshi, Okin, Lee, and Kathail to create a device tree describing the hardware devices in the computer system with the open firmware, thus indicating marking the spare processor by an open firmware. 'A person of ordinary skill in the art would have been motivated to combine the teachings because Lee discloses using open firmware (see column 1 lines 26-29) and Kathail discloses a device tree is a known feature of open firmware (see column 25 lines 33-35).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See Form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emerson C. Puente whose telephone number is (571) 272-3652. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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